AMENDMENTS TO THE CLAIMS

1. (Canceled)

2. (Original) An MPEG data processing circuit which processes inputted MPEG data to produce outputted MPEG data, comprising:

V-ES detecting section which judges said inputted MPEG data to output video stream status signal indicating output status of system stream data and video elementary data within said system stream data;

a memory which stores non-video elementary data portion from said V-ES detecting section;

a barrel shifter which divides video elementary data portion from said V-ES detecting section into bit units and which stores the bit units of said video elementary data portion;

a variable length decoder which is connected to an output of said barrel shifter;

a data replacing section which is connected to an output of said variable length decoder;

a variable length encoder which is connected to an output of said data replacing section;

a bit packer section which is connected to an output of said variable length encoder;

a data combining section which combines an output of said bit packer section and an output of said memory to produce said outputted MPEG data in an original order;

a control section which controls input and output of data in said barrel shifter and said data replacing section based on a first control signal from said V-ES detecting section, a signal from said variable length decoder, and a signal from said data combining section; and

a memory control section which controls input and output of data in said memory based on said first control signal from said V-ES detecting section and which outputs a second control signal to said control section.

3. (Original) An MPEG data processing circuit as claimed in claim 2, wherein said memory control section refers an amount of remaining data in said memory in a case that not fewer than one byte of video data stream are outputted from said V-ES detecting section, said memory control section making data in said barrel shifter be outputted from said data combining section when no data are stored in said memory.

4. (Original) An MPEG data processing circuit as claimed in claim 2, wherein said data replacing section is an electronic watermark inserting section, said MPEG data processing circuit further comprising an electronic watermark detecting section which is connected to an output of said variable length decoder.

5. (Original) An MPEG data processing circuit as claimed in claim 3, wherein said data replacing section is an electronic watermark inserting section, said MPEG data processing circuit further comprising an electronic watermark detecting section which is connected to an output of said variable length decoder.

6. (Original) An MPEG data processing circuit as claimed in claim 2, further comprising:

a preceding output length storing section for storing numbers of remaining data stored in said barrel shifter to be precedingly outputted therefrom with the numbers of remaining data being kept therein; and

a fraction length storing section for storing difference obtained by subtracting a stored value in said preceding output length storing section from numbers of data outputted in response to data, at first, inputted to said barrel shifter after the preceding output.

7. (Original) An MPEG data processing circuit as claimed in claim 3, further comprising:

a preceding output length storing section for storing numbers of remaining data stored in said barrel shifter to be precedingly outputted therefrom with the numbers of remaining data being kept therein; and

a fraction length storing section for storing difference obtained by subtracting a stored value in said preceding output length storing section from numbers of data outputted in response to data, at first, inputted to said barrel shifter after the preceding output.

8. (Original) An MPEG data processing circuit as claimed in claim 4, further comprising:

a preceding output length storing section for storing numbers of remaining data stored in said barrel shifter to be precedingly outputted therefrom with the numbers of remaining data being kept therein; and

a fraction length storing section for storing difference obtained by subtracting a stored value in said preceding output length storing section from numbers of data outputted in response to data, at first, inputted to said barrel shifter after the preceding output.

9.-10. (Canceled)

11. (Original) A method of controlling an MPEG data processing circuit for use in controlling said MPEG data processing circuit as claimed in claim 8, said method comprising the steps of:

dividing an MPEG data stream inputted to said MPEG data processing circuit into non-video elementary data portion and video elementary data portion;

primary storing said non-video elementary data portion in said memory;

secondary storing said video elementary data portion in said barrel shifter;

replacing a value of a predetermined position of data group obtained by variable length decoding said video elementary data portion stored in said barrel shifter with a desired value;

obtaining a processed data block by variable length encoding the replaced data group;

combining said processed data block and said non-video elementary data portion stored in said memory with each other in an order of input to be outputted as an MPEG data stream; and

storing numbers of remaining data stored in said barrel shifter in said preceding output length storing section and outputting the numbers of remaining data from said barrel shifter with the remaining data being kept therein, when it is detected that said memory is full, that said data combining section is condition waiting for an input, that all of said variable length decoder, said electronic watermark inserting section, and said variable length encoder have no data, that said barrel shifter has remaining data, and that the remaining data cannot be decoded.

12. (Original) A method of controlling an MPEG data processing circuit for use in controlling said MPEG data processing circuit as claimed in claim 8, said method comprising the steps of:

dividing an MPEG data stream inputted to said MPEG data processing circuit into non-video elementary data portion and video elementary data portion;

primary storing said non-video elementary data portion in said memory;

secondary storing said video elementary data portion in said barrel shifter;

replacing a value of a predetermined position of data group obtained by variable length decoding said video elementary data portion stored in said barrel shifter with a desired value;

obtaining a processed data block by variable length encoding the replaced data group;

combining said processed data block and said non-video elementary data portion stored in said memory with each other in an order of input to be outputted as an MPEG data stream; and

controlling said barrel shifter, in a case that said barrel shifter has remaining data, to output the remaining data therefrom, when it is detected that said MPEG data stream is not inputted for a certain time.

13. (Original) A method of controlling an MPEG data processing circuit for use in controlling said MPEG data processing circuit as claimed in claim 8, said method comprising the steps of:

dividing an MPEG data stream inputted to said MPEG data processing circuit into non-video elementary data portion and video elementary data portion;

primary storing said non-video elementary data portion in said memory;

secondary storing said video elementary data portion in said barrel shifter;

replacing a value of a predetermined position of data group obtained by variable length decoding said video elementary data portion stored in said barrel shifter with a desired value;

obtaining a processed data block by variable length encoding the replaced data group;

combining said processed data block and said non-video elementary data portion stored in said memory with each other in an order of input to be outputted as an MPEG data stream; and

controlling said barrel shifter, in a case that said barrel shifter has remaining data, to output the remaining data therefrom, when a notice of finish of input of a unit of said MPEG data stream is inputted from the outside of said MPEG data processing circuit.

14. (Previously Presented) A processing circuit for a data stream including video data and non-video data which inputs and processes said data stream comprising:

a split unit dividing said input data stream into said video data and said non-video data; and

a primary store that stores said video data in sequence; and

a secondary store that stores data length of said video data written in said primary store and said non-video data in order of said data stream being input; and

an image processing unit for processing said video data read out of said primary store; and

a data combining unit wherein video data after image processing and said non-video data output are combined in an original order by reading out data length of said video data and said non-video data from said secondary store in stored order and combining video data processed by said image processing unit when the length of said video data is being read out.

15. (Canceled)